

**IN THE CLAIMS**

1-11. (Currently Canceled)

12. (Currently Amended) An array of planar T-RAM cells comprising:  
a plurality of T-RAM cells, said plurality of T-RAM cells being arranged in an array and  
fabricated over a substrate, each of said plurality of T-RAM cells including a first buried vertical  
thyristor and a second device horizontally stacked pseudo-TFT transfer gate, said first device  
thyristor being buried underneath said second device transfer gate, wherein said second device  
transfer gate covers the entire top surface of said first device thyristor, and further wherein the  
top surface of said second device transfer gate forms a planar top surface of each said T-RAM  
cell.

13. (Currently Canceled)

14. (Original) The array according to Claim 12, wherein each of the plurality of  
T-RAM cells has a size of less than or equal to  $8F^2$ .

15. (Previously Amended) The array according to Claim 12, wherein said  
substrate is a semiconductor SOI or bulk wafer.

16. (Previously Amended) The array according to Claim 13, wherein a base of  
said thyristor is surrounded by a surrounded gate.

17. (CurrentlyAmended) The array according to Claim 12, wherein said planar top surface of each T-RAM cell provides for simplified fabrication of ~~metal~~ wirings wordlines, said wirings wordlines being fabricated over said planar top surface of said T-RAM cells, said wirings wordlines for interconnecting said T-RAM cells.

18-30. (Currently Canceled)

31. (New) An array of planar T-RAM cells comprising:  
a plurality of T-RAM cells, said plurality of T-RAM cells being arranged in an array and fabricated over a substrate, each of said plurality of T-RAM cells including a buried vertical thyristor and a horizontally stacked pseudo-TFT transfer gate, said thyristor being buried underneath said transfer gate, said transfer gate covering a part of a top surface of said thyristor, the top surface of said transfer gate forming a planar top surface of each said T-RAM cell.